A High Performance Digital Hearing Aid for Advanced Sound Processing Research

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Abstract—A portable programmable digital sound processor has been developed for advanced hearing aid research. The system features a fully programmable 24-bit Digital Signal Processor (DSP), a low-noise programmable-gain dual preamplifier, a 16/20-bit stereo audio CODEC, a dual power amplifier, and a 128 kB programmable erasable read-only memory (PEROM). Two hearing aid microphones and two receivers may be connected simultaneously to the processor allowing true binaural and microphone array processing. The processor is powered by a single AA-size cell and is pocket-sized and lightweight. The processor is currently being used to develop and assess several new hearing aid sound processing schemes that were not feasible in previous, less powerful portable devices.

Index Terms—Digital signal processor, hearing aid, binaural, microphone array, dual channel.

I. INTRODUCTION

Hearing aids are the most common auditory prostheses fitted to people with a hearing loss. Despite recent advances in digital hearing aid technology, many hearing aid users do not hear well in noisy environments and may occasionally experience uncomfortable loudness levels. Algorithms such as directional microphone arrays [1] and real-time loudness models [2] may be of assistance in these situations. Advanced hearing aid research involves investigating how such algorithms can be used to improve the performance of hearing aids in all acoustic conditions.

Commercially available hearing aids are generally not suitable for advanced hearing aid research. This is because they are not fully programmable, their architecture is inflexible and optimised for one specific algorithm, their acoustic dynamic range is not suitable for some algorithms, and they lack the computational power required for the quick implementation of unoptimised code. A previously described portable digital sound processor, referred to as the P-DSP [3], and a modification known as the P-DSP/HA [4], were much larger, heavier and had a much shorter battery life than commercially available hearing aids. These factors were inconvenient to the hearing aid user, and may have reduced the amount of experience gained with new sound processing schemes in everyday conditions away from the laboratory. A later digital sound processor [5] was smaller, lighter and more powerful, but required a specialised cell chemistry and could only accept one microphone signal. A low-power DSP recently developed for hearing aid research [6] had an inadequate word length and amount of on-chip memory for advanced algorithms. Therefore, a small, light, cosmetically appealing, highly flexible, fully programmable, and powerful portable digital sound processor is required for the rapid development, modification, and evaluation of advanced hearing aid sound processing schemes in everyday conditions. The processor should avoid the limitations of previous designs for hearing research, such as those mentioned above. A digital sound processor that meets all of the requirements of advanced hearing aid research has been developed, which henceforth will be referred to as SHARP (Stereo Hearing Aid Research Processor).

II. HARDWARE DESIGN

A diagram of the major components of the SHARP circuit is shown in Fig. 1. The SHARP circuit is centred on the fully programmable Motorola DSP56309 DSP, which has enough memory and computational power to run advanced hearing aid algorithms. This DSP is rated at one million instructions per second (MIPS) per MHz of core clock frequency for single instructions, and can process up to 3 instructions in parallel during one clock cycle. An on-chip phase-locked loop multiplies the quartz crystal frequency to set an appropriate internal core operating frequency of up to 80 MHz. The word length is 24 bits, long words of 48 bits are supported, and the results of calculations are stored in two 56-bit accumulators. The total internal memory is 34 kilowords, eliminating the need for relatively slow external random access memory. The on-chip peripherals include three serial ports, a parallel port,
provide suitable clocks for a CODEC and to support high-speed asynchronous RS-232 communications with a host computer. Algorithms and data are stored in a PEROM that is DSP-writable with system level voltages. The DSP can boot from either the PEROM or the host computer via an external RS-232 interface.

The 80 dB dynamic range that is required for some types of hearing loss is provided by a dual low-noise programmable-gain microphone preamplifier, a 16/20-bit stereo audio CODEC, and a single-ended dual power amplifier. Thin, shielded, skin-coloured cables connect the processor to one or two behind-the-ear (BTE) packages, which may contain up to two microphones and one receiver (a miniature speaker) in each package. The preamplifier gain is DSP programmable between 6 and 30 dB. The output of the dual preamplifier is connected to the A/D converter of the stereo CODEC, which digitises the amplified microphone signals into 16 or 20-bit samples. The sample length is controlled by the DSP, which also provides the clocks required for the CODEC timing circuit and the serial port data link. The sampling rate is determined by the DSP serial port clocks and may be between 4 and 48 kHz per channel. Samples received by the CODEC’s D/A converter from the DSP are converted into analogue signals that are fed into the dual power amplifier input via two trimpots. The trimpots are used to select the maximum output level in each ear so that it remains below a level that could cause discomfort to the hearing aid user. The power amplifier is designed to drive receivers with an impedance as low as 100 Ω over a frequency range of 100 Hz to 10 kHz.

The processor is housed in a small (91 × 61 × 19 mm), light (90 g), and ergonomic body-worn box developed by Cochlear Limited for a commercially available cochlear implant speech processor. The box houses a three-way program selection switch, a rotary parameter adjustment control, an external audio input socket, a serial interface socket, and two light-emitting diodes (LEDs). The positions of the switch and rotary control are read periodically by the DSP, which also addressing. The serial ports may be configured to drives the LEDs directly. The functions of the program mode switch, rotary control, and LEDs are fully programmable. These controls are typically used to select alternative frequency response shapes (program mode switch), adjust the volume (rotary control), and indicate a low battery level (LEDs).

The power source may be any single primary or rechargeable AA-size cell with a working voltage between 0.7 and 3.3 volts. The cell voltage is boosted to 3.3 volts by a low-noise DC-to-DC converter IC. The DC-to-DC converter output is split into separate regulated 3.0 volt analogue and digital supplies to minimise digital noise in the audio circuit. When the cell reaches the end of its life the DSP is safely held in the reset state by a voltage monitor IC. The DC-to-DC converter IC also includes an A/D converter that is periodically read by the DSP to monitor the cell voltage and the position of the rotary control. Therefore, the DSP can shut down in a controlled manner just before the cell reaches the end of its life.

DSP and PC software has been developed to program and control the processor via a PC serial port at 115.2 kb/s using an external RS-232 interface box. This software allows program parameters and coefficients to be adjusted while the processor is running a sound-processing algorithm without the need to reboot the DSP. Therefore, program modifications can be assessed immediately while the hearing aid user is using the device in the laboratory.

III. PERFORMANCE

A test program was run to measure the useable dynamic range of the audio section of SHARP. The DSP core clock frequency was set to 8.192 MHz and the CODEC was sampling 16-bit samples at a rate of 16 kHz per channel. The preamplifier and power amplifier trimpots were both set to maximum gain, resulting in a total electrical gain of 34 dB. The BTE connected to SHARP contained a Knowles low noise EM-3456 microphone and a Knowles high output CI-2762 receiver. The measurements were made with a Brüel & Kjær Type 2235 sound level meter connected to a Brüel & Kjær Type 4157 ear simulator. The receiver was coupled to the ear simulator via 21 mm of 2 mm internal diameter plastic tube and the earhook of the BTE. During the noise floor measurements the microphone port was sealed and the DSP transmitted samples back to the CODEC unmodified. During the maximum output measurements the DSP generated full-scale output tones. Figure 2 shows the maximum sound pressure level (SPL) measured at the receiver, the equivalent input noise level at the preamplifier, and the output dynamic range in 1/3rd-octave bands. The equivalent input noise level closely follows the specified microphone noise level. Therefore, the measured noise floor is dominated by the microphone noise. The average output dynamic range of the 1/3rd-octave bands was 82 dB.
To demonstrate the computational performance of
the processor when running an advanced hearing aid
algorithm, a loudness model for cochlear hearing loss
was implemented. This model estimates the
loudness contributed by each frequency component of
a sound. In the normal cochlea (inner ear), mechanical
filtering converts each acoustic frequency to a position
of maximal excitation. The computational model
simulates this process by means of a bank of band-pass
filters having overlapping frequency responses. Each
filter corresponds to a unique position in the cochlea.
The model computes the specific loudness (i.e. the
loudness contributed by the excitation at each position,
or at each corresponding frequency) by an appropriate
transformation of the outputs of the filters. If required,
the total loudness can also be calculated by integrating
the specific loudness function across frequency (or
across position in the cochlea). Furthermore,
parameters of the model can be selected to estimate
the loudness perceived by a listener with a
sensorineural hearing impairment, instead of the
loudness perceived with normal hearing. Such
loudness modelling may have applications in advanced
hearing aids, because it is generally desirable to be
able to amplify sounds for aid-users in a way that
results in near-normal perception of loudness. For a
loudness model to be of practical use in a hearing aid,
it is essential that the complex numerical computations
be carried out in real time.

The loudness model was implemented in the
SHARP with the DSP core clock frequency set to
16.384 MHz and a sampling rate of 16 kHz per
channel. An estimate of the sound spectrum detected
by the microphone was obtained every 4 ms (64
samples) with a 128-point Fast Fourier Transform
(FFT) using a 256-point Hanning window that was
folded into a 128-point FFT input buffer. This
overlap-add windowing technique [8] was chosen
because it produces FFT bins with steeper slopes than
those achieved with a conventional 128-point window.
The input power spectrum was then calculated, and the
power values scaled up so that the maximum input
level corresponded to the maximum numerical value in
the DSP. After scaling, the numerical dynamic range
of the power values was 69.2 dB. The loudness model
was then executed with the scaled FFT power
spectrum as its input.

The output of the loudness model for an 80 dB SPL
tone at 1 kHz and a hypothetical 40 dB
hearing loss at all frequencies is shown in Fig. 3. For
comparative purposes, the specific loudness calculated
by a more precise PC implementation of the model is
also shown. This example demonstrates that the output
of the real-time model implemented in the SHARP
closely approximates that of the non-real-time
implementation. The total DSP processing time to
compute the loudness model was 1.076 ms, while the
processing time for the windowing, FFT, power
spectrum calculation, and inverse FFT was 0.884 ms.
Therefore, if the loudness model was calculated after
every FFT, 51% of the available processing time
would remain for other tasks. The power consumption
of the SHARP during the test was 160 mW, which
should result in a battery life of approximately 15
hours when using a high quality alkaline cell. To
simulate the effect of performing other tasks, the
loudness model was executed twice after every FFT.
This resulted in 76% of the available processing time
being used and a slightly greater power consumption
of 185 mW.

IV. DISCUSSION
The SHARP platform is powerful enough for advanced hearing aid algorithms to be developed with minimal code optimisation. Therefore, the researcher's time is not wasted optimising code that shows little potential. When optimising code, the researcher can easily test the effectiveness of the scheme after making the approximations required for the implementation of the algorithm in a commercial device. Some commercially available digital hearing aids contain a co-processor that performs the spectral analysis of the sound signal [9]. Therefore, the hearing aid's DSP can dedicate almost all of its processing power to the sound processing scheme, which may be from 1 to 4 MIPS.

The spectral analysis and the loudness model for cochlear hearing loss that were implemented form the foundation of an advanced sound processing scheme. The spare processing power may be used to execute the loudness model with different parameters, collect statistics, save data, perform an FFT on the second audio channel, implement a directional microphone array, or calculate non-linear gain equations. The second loudness calculation could be for normal or impaired hearing, depending on whether the goal of the processing scheme was to restore normal loudness in an impaired ear, or to balance the loudness in two unequally impaired ears. The relationship between loudness and SPL is non-linear, and varies greatly among hearing-impaired people. Also, an increase in the total SPL does not always translate to an increase in loudness [10]. Therefore, loudness models can be more useful than SPL measurements alone in meeting common goals of hearing aid schemes, such as normalising or equalising loudness, maintaining good audibility, and avoiding uncomfortable loudness.

Multi-microphone systems can be used to implement algorithms such as directional microphone arrays and spatial binaural sound processing. With many common types of hearing aids, spatial acoustic cues are lost and sounds seem to emanate from inside the hearing aid user's head. These cues may be restored by advanced algorithms that model the time delays and phase shifts created by the pinna (outer ear) and the resonances of an open ear canal. The restoration of spatial acoustic cues may improve discrimination between two competing sound sources, as well as creating a more natural sounding hearing aid.

V. CONCLUSION

A portable programmable digital sound processor has been designed for the rapid development and assessment of advanced hearing aid algorithms. It features two independent low-noise audio channels, a fully programmable DSP, a DSP-writable PEROM, and is powered by a single AA-size cell. The processor is housed in a small, light, and cosmetically appealing box that is connected to two BTEs via thin shielded cables. The processor does not share the practical limitations of previous designs for hearing research, such as short battery life and excessive size and weight. These practical aspects should encourage the use of the device in many situations commonly encountered outside the laboratory. The processor has the flexibility to support true binaural and multi-microphone schemes, and the computational power to execute advanced algorithms such as a loudness model for cochlear hearing loss.

Current and future research with the processor includes an investigation into the use of loudness models in hearing aids, and the development of algorithms to improve speech perception in noisy environments.

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VII. REFERENCES